

FIG. 1

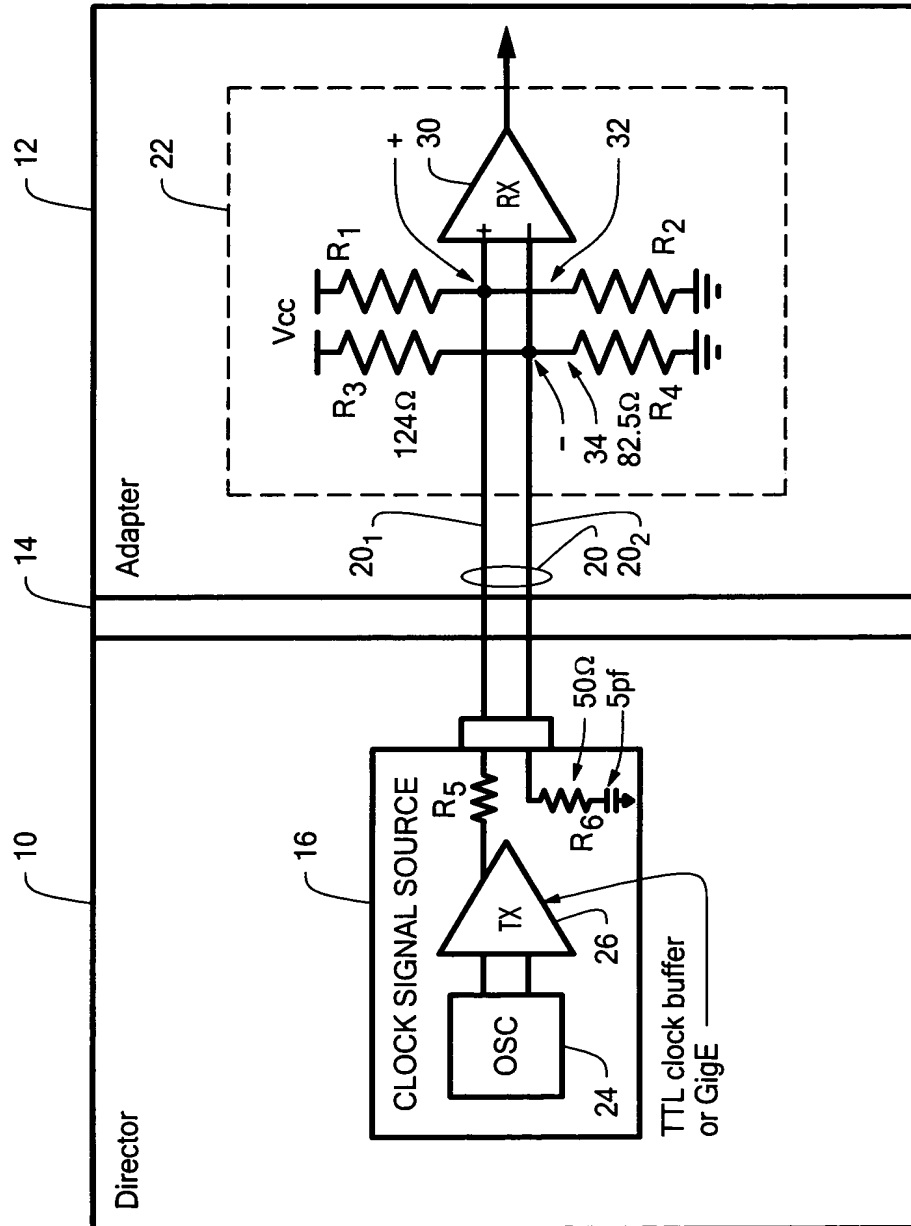


FIG. 2

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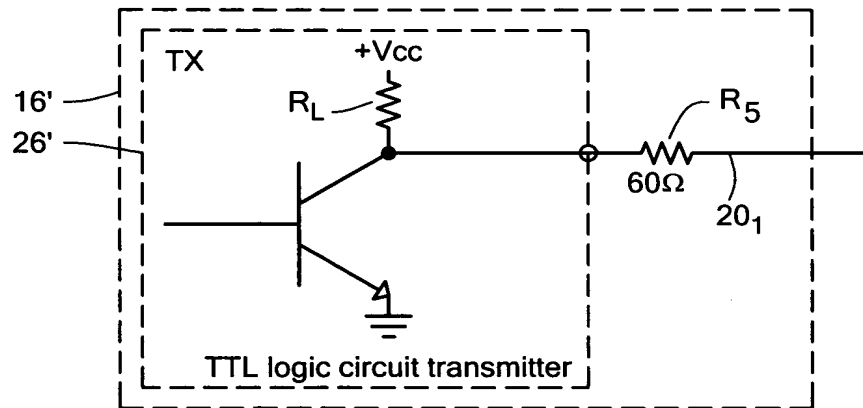


FIG. 3

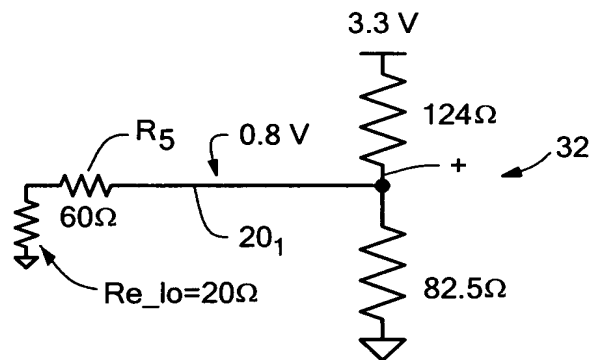


FIG. 4A

TTL output low

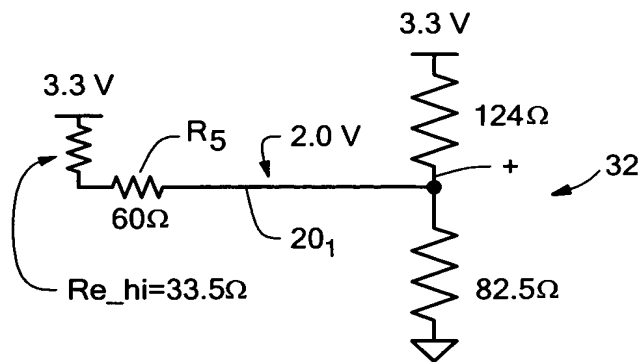


FIG. 4B

TTL output high

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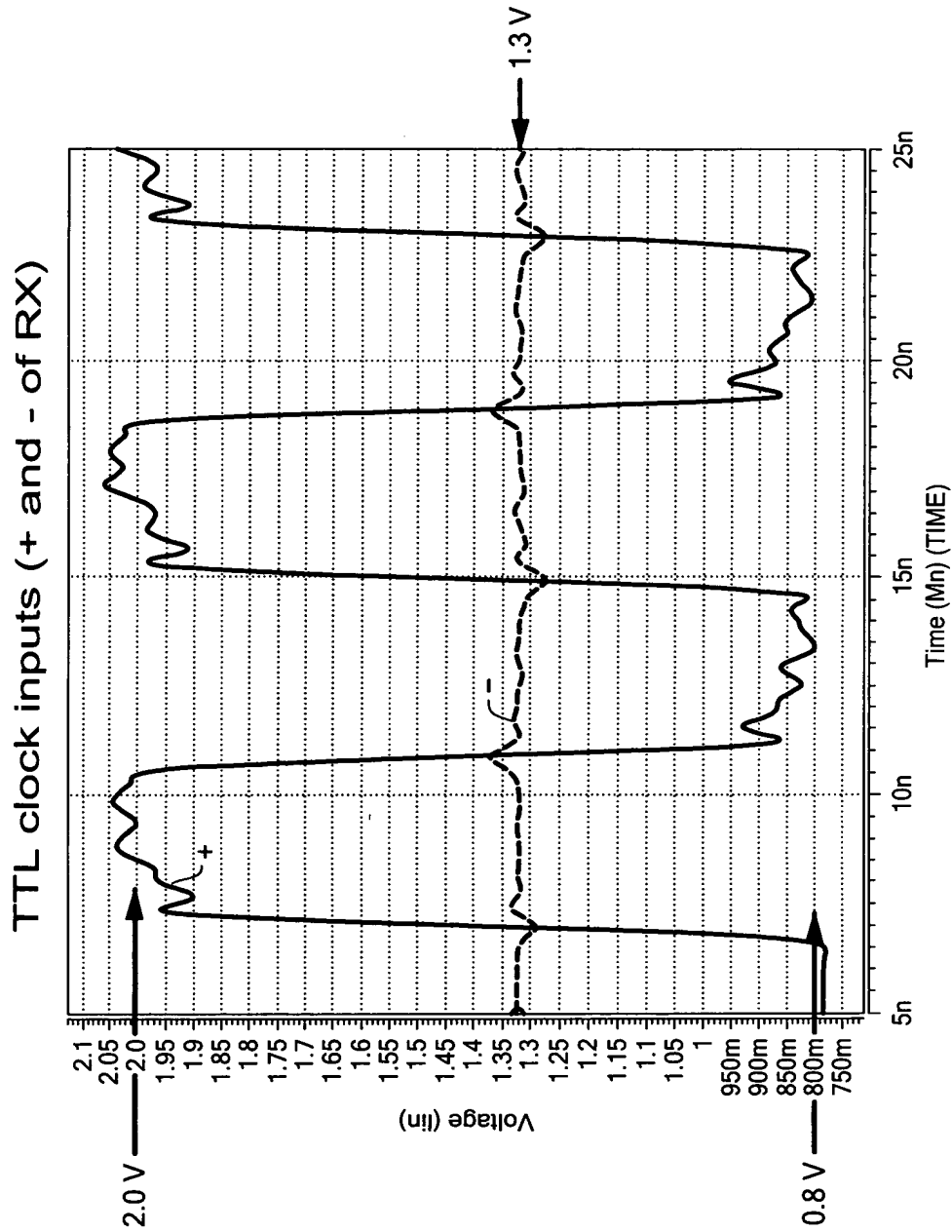


FIG. 5

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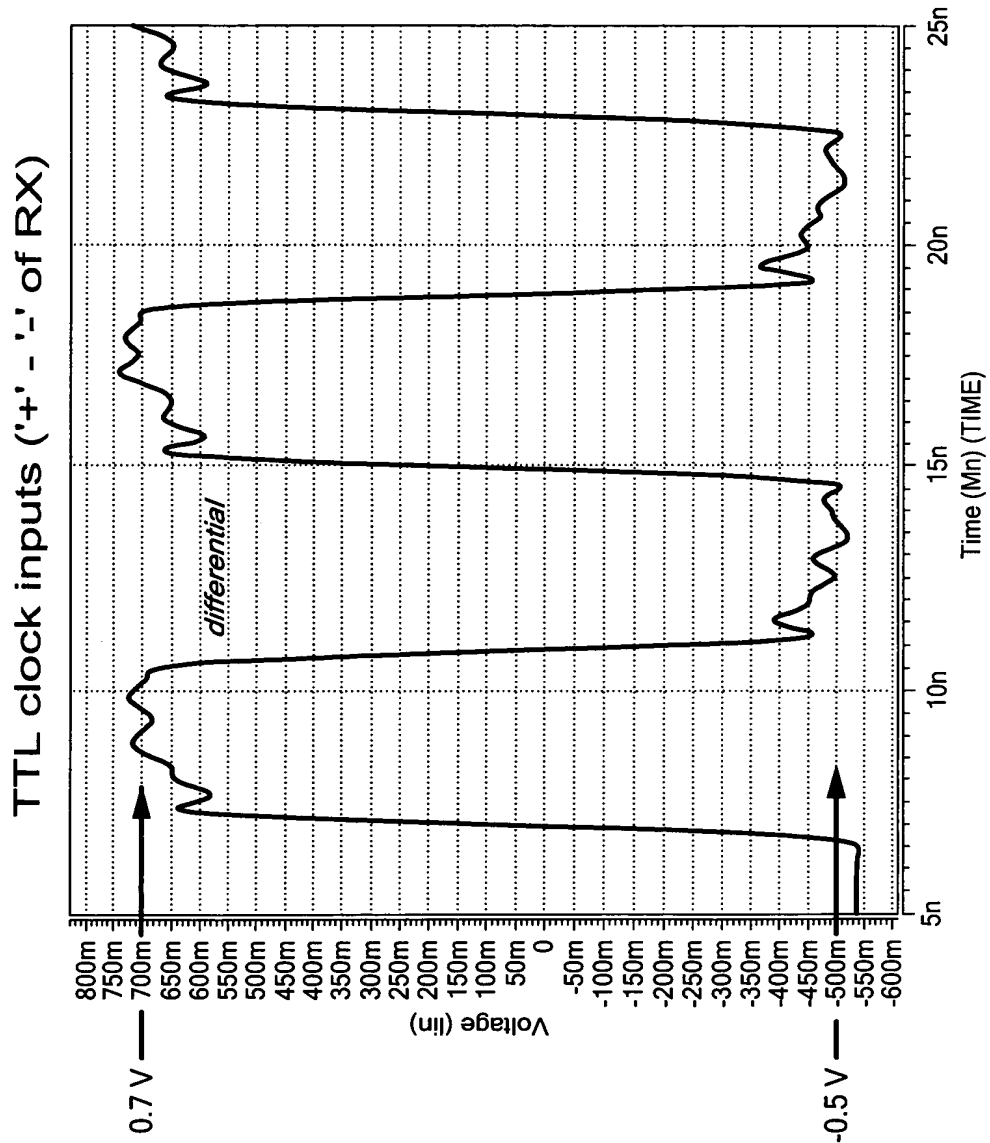


FIG. 6

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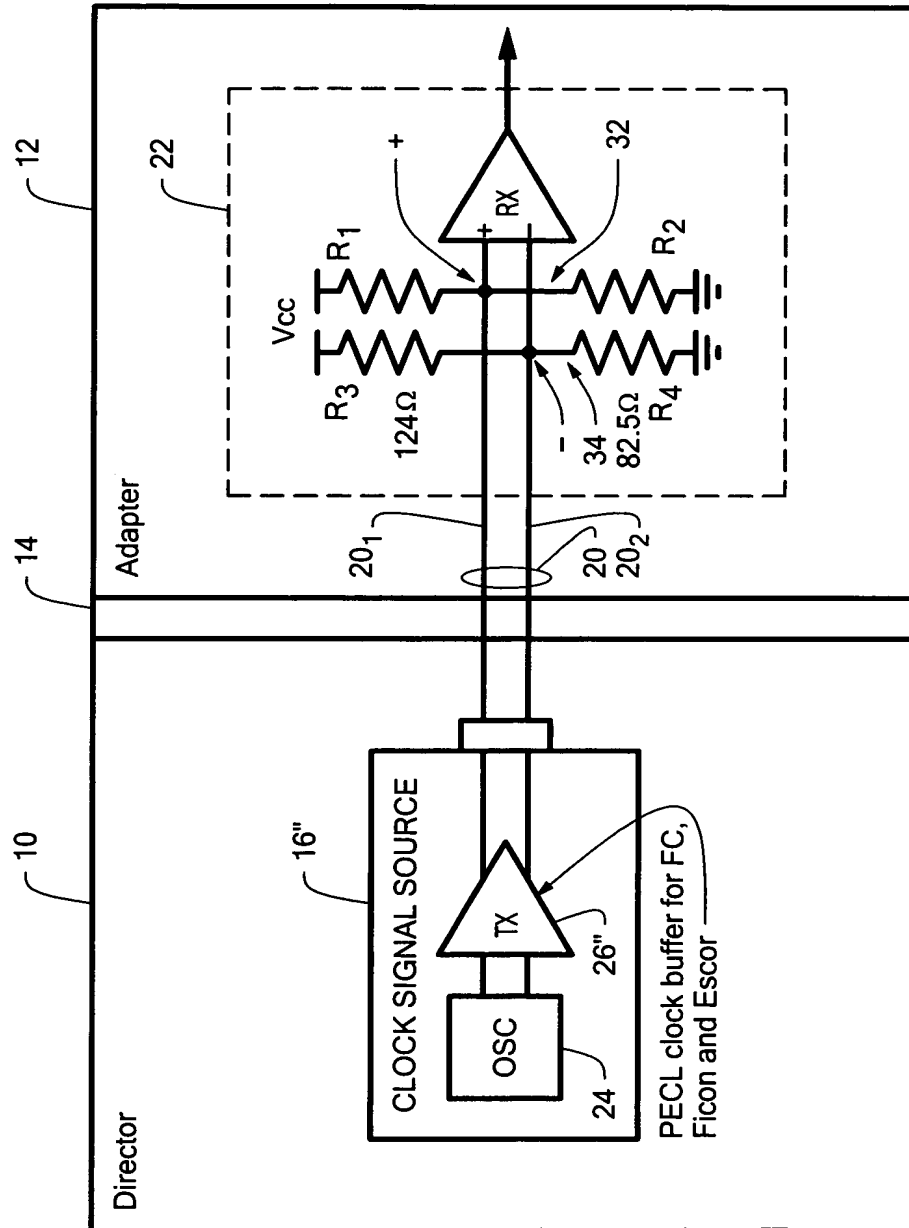


FIG. 7

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PECL clock input signals (+ and - of RX)

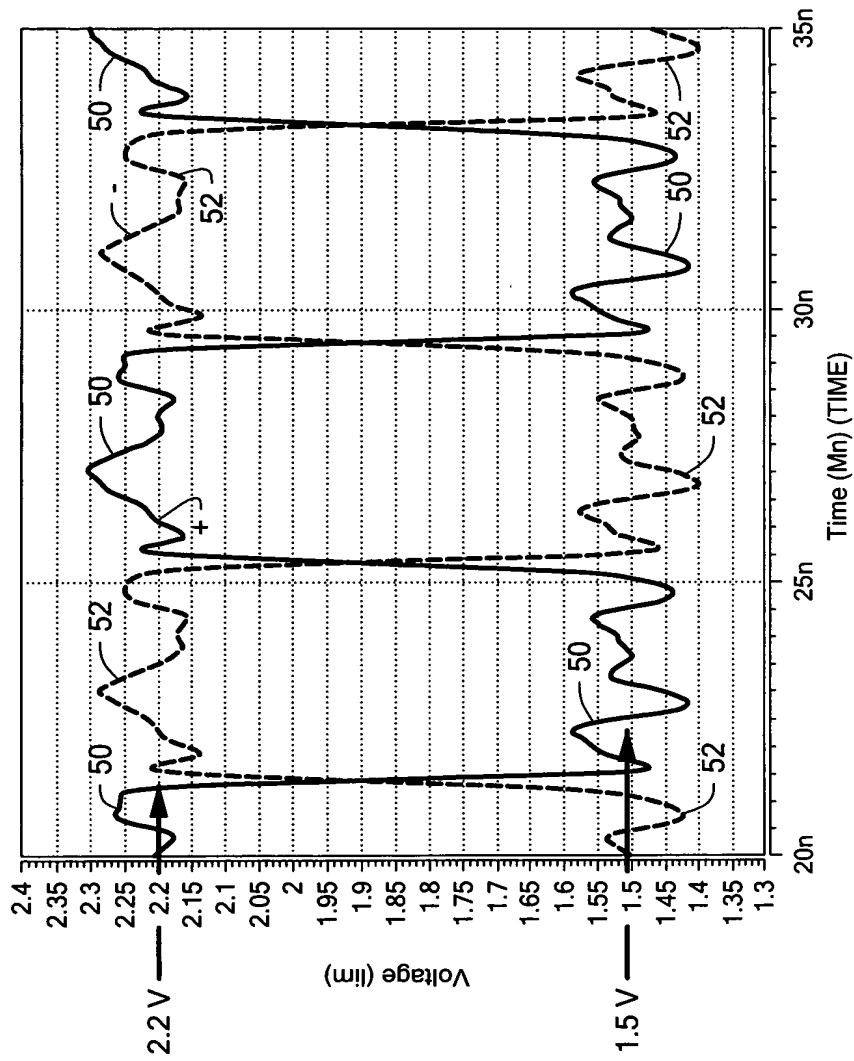


FIG. 8

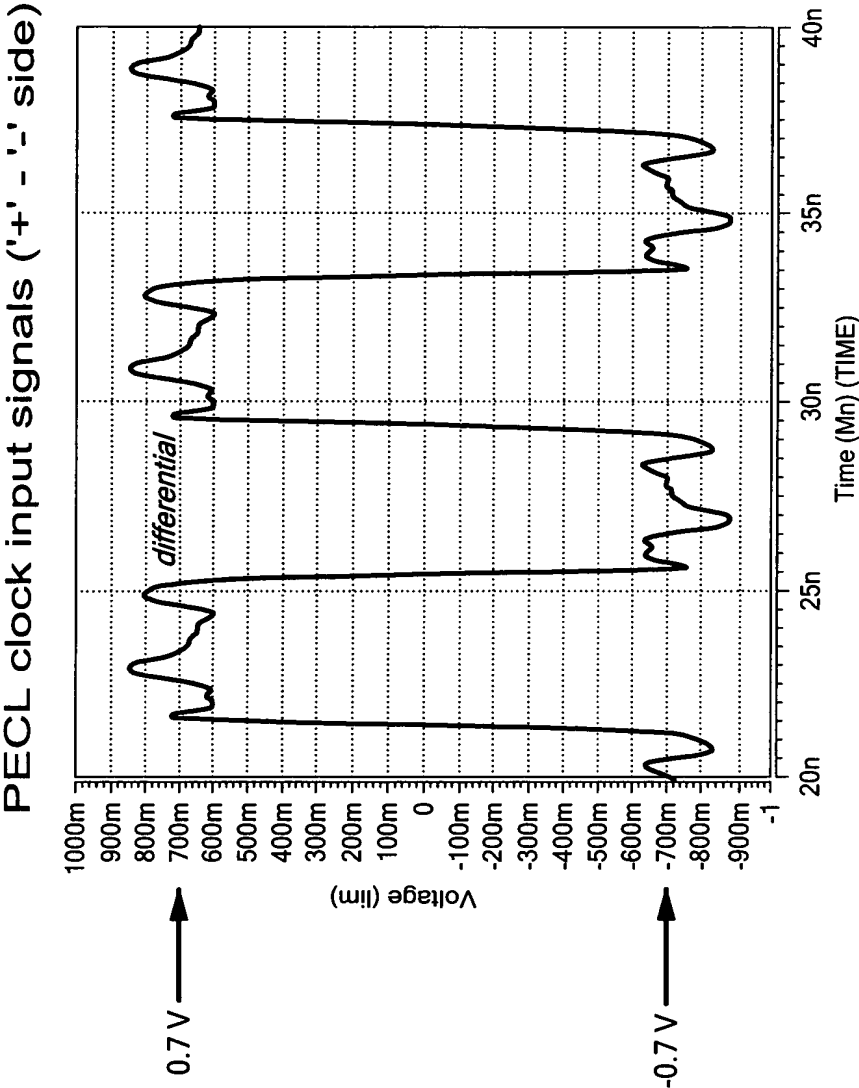


FIG. 9